Serial Number
98 5-141

SA


## ABSTRACT

A Memory Interface and Video Attribute Controller (MIVAC) is inserted between a dynamic RAM (DRAM) capable of a consecutive data read operation, such as the operation associated with the static column mode, page mode, or nibble mode, and a graphic processor to provide a parallel data processing. A serial data transfer is executed on each data bus between the MIVAC and the DRAM, whereas parallel data transfer is conducted between the MIVAC and the graphic processor. As a result, the graphic processor can be configured with a reduced number of DRAMs so that the graphic processor operates without paying attention to the consecutive data read mode of the DRAM.


EA